

Energy-Efficient Power Conversion Architectures

6th May 2010



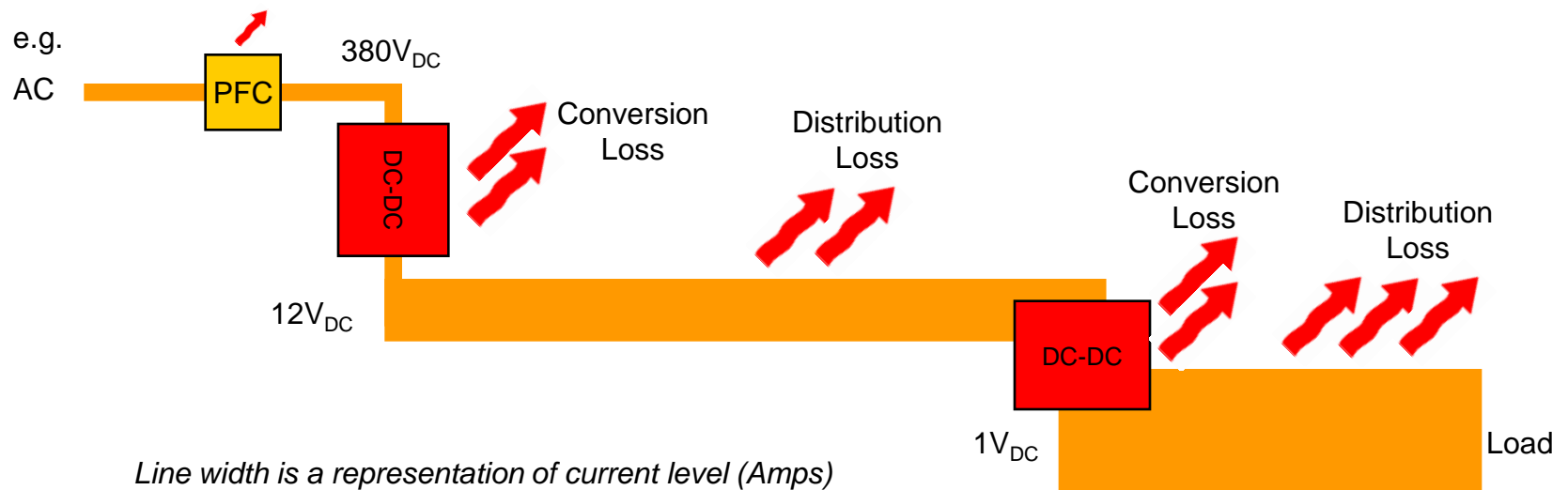
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The Cost of Power Inefficiency

- Going from 'A' to 'B'
 - From AC to the load – the complete chain
- Power is 'lost'
 - #1: Along the way (distribution losses, connector losses)
 - #2: Stepping down (conversion losses)
- Leading to more heat and more cost





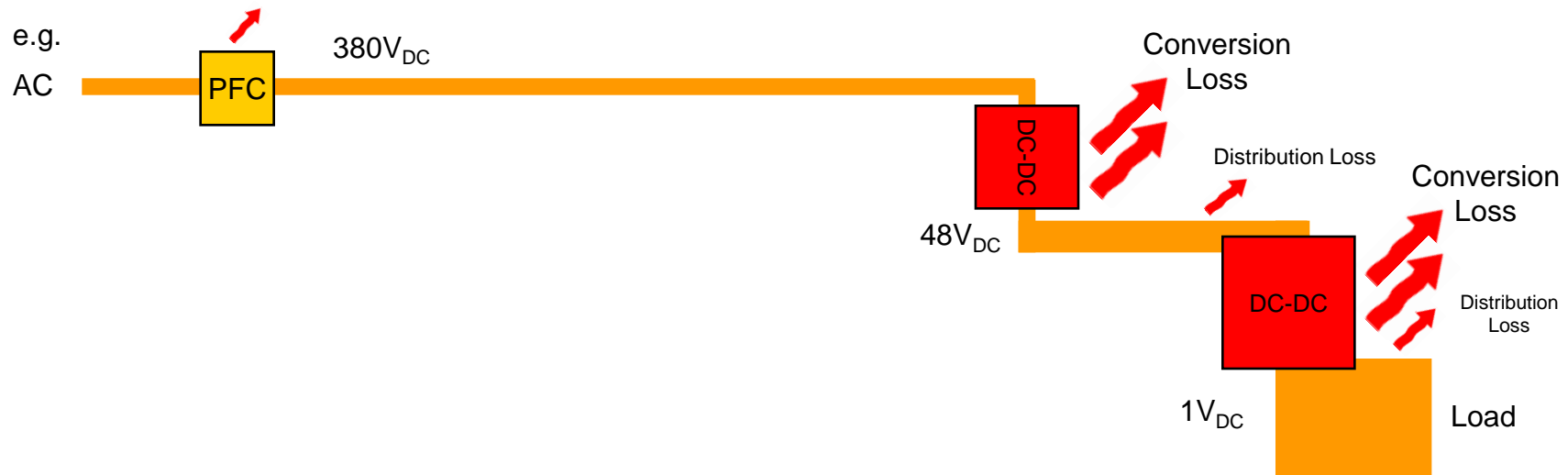
More Heat, More Cost

- More Heat
 - Larger, heavier heatsinks
 - More air-conditioning
 - Lower reliability
 - Larger, heavier systems, etc.
- Higher Cost
 - Cost of the cooling system
 - Cost of electricity year after year (\$/MWhr)
 - Cost of fuel (airborne systems)
 - ‘Total Cost of Ownership’ (TCO)



High Efficiency Power Distribution

- In large systems, transmission/distribution loss is a problem
 - Power loss is related to current² ($P_{LOSS} = I^2R$)
 - So, keep the voltage high (current low), to as close to the load as possible
 - 12V is very high loss (connector loss, pcb distribution loss, etc.)
 - 48V is 16x better (i.e. 16x lower losses) than 12V
 - 380V is 1,000x better than 12V





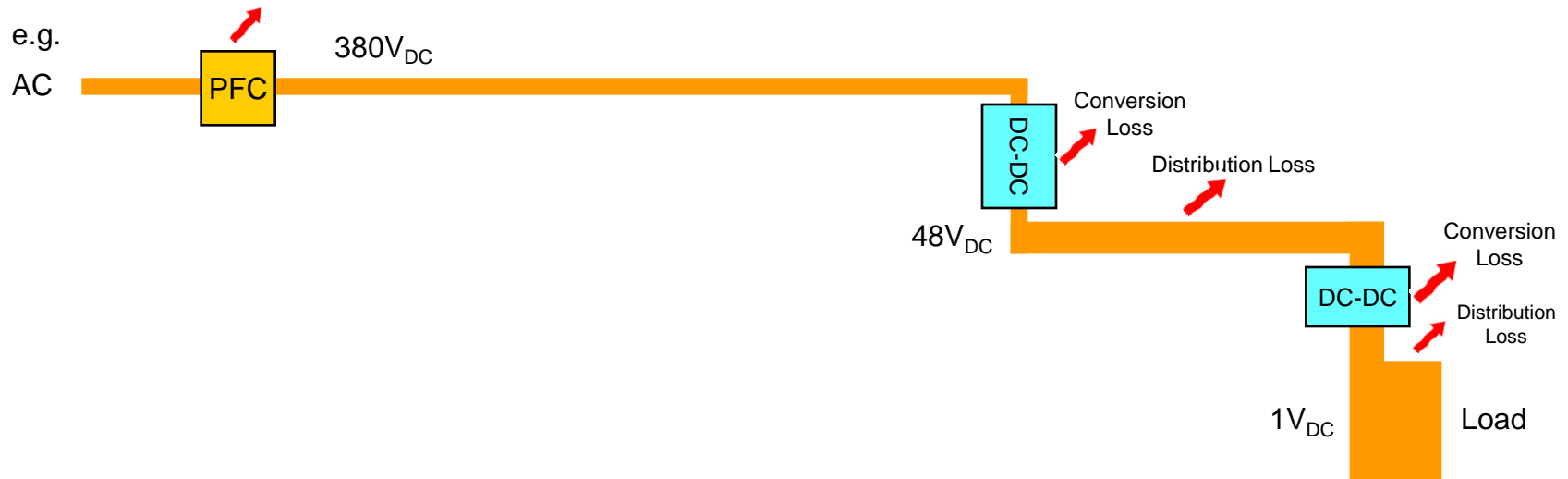
HVDC Distribution Today:

- 350-400V in *datacenters*
 - Telecom (NTT, Hitachi, NEC, etc.)
 - Computing (Hitachi, LBNL, Intel, etc.)
- 350-400V in *rack*
 - Computing (IBM Power6, Power 7, Cray CX1, Dell LC, Verari, etc.)
- 270V in *airframe*
 - Aerospace (Raytheon, Lockheed Martin, Harris, etc.)
- 48V in *rack or shelf*
 - Telecom (Huawei, Alcatel, etc.)
 - Computing (IBM Blue Gene/P, etc.)
 - ATE (Advantest, Teradyne, KLA, etc.)
 - Solid-state (LED) Lighting / Display



High Efficiency Power Conversion

- Power conversion efficiency is driven by:
 - Topology
 - High efficiency building blocks – smaller, less heatsinking, *even closer to the load*
 - Minimum conversion stages
 - Eliminate duplicate functions
- Choice of Topology is driven by:
 - System architect's understanding of Total Cost of Ownership
 - Time to design / time to market / availability of conversion building blocks
 - System-wide benefits, e.g.
 - Light-load efficiency
 - Soft-switching / high frequency operation reduces filter size / loss / complexity
 - Low impedance converters enabling bulk capacitance elimination





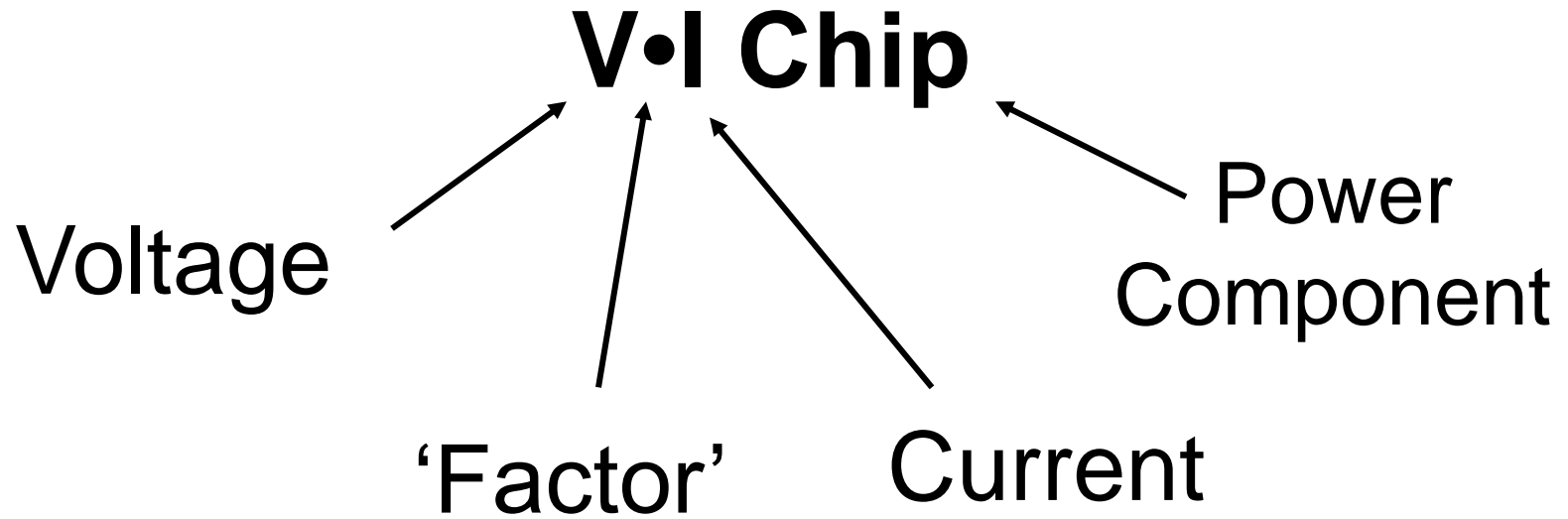
Factorized Power Architecture (FPA) and V·I Chips

- A power supply has 2 functions: Regulation & Voltage Transformation
- In an old, traditional system (e.g. flyback, forward, half-bridge)
 - Regulation & Voltage Transformation are connected
 - Difficult to improve performance
 - Consolidated blocks lead to poor **system** performance
- In Factorized Power Architecture (FPA)
 - Regulation & Voltage Transformation are **separated** ('Factorized')
 - Easy to improve performance
 - Good system performance
 - Low distribution loss
 - Reduces duplicated functions
 - Reduces power dissipation at the load
- FPA uses V·I Chips
 - Small, powerful components
 - Highest power density
 - High efficiency
 - Fast, flexible design
 - Good transient response





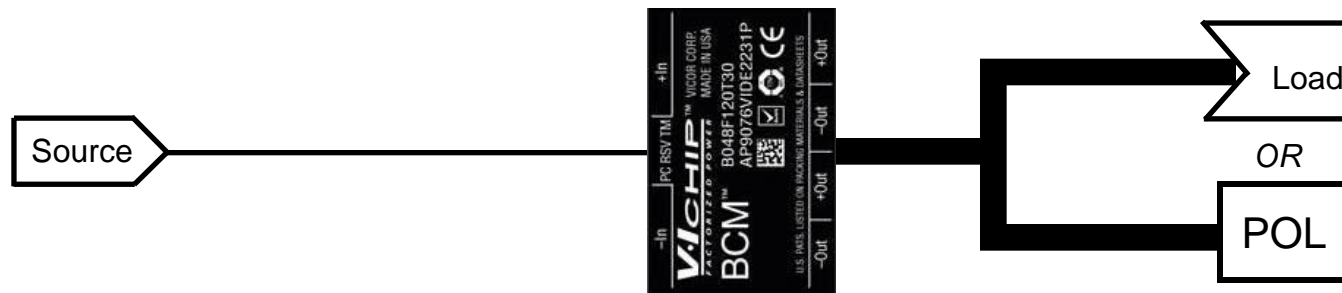
V·I Chip?



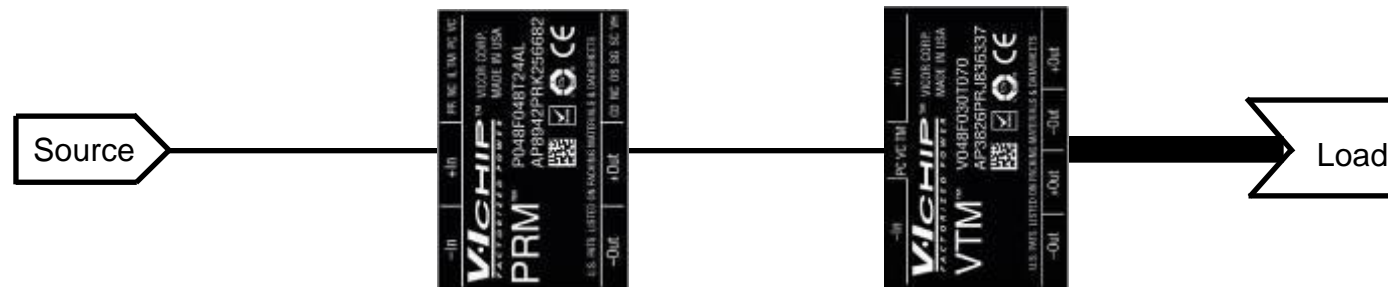


DC-DC Conversion

- Non-regulated = BCM (Bus Converter)
 - 380V / 350V / 48V_{IN} converters



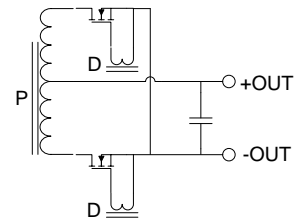
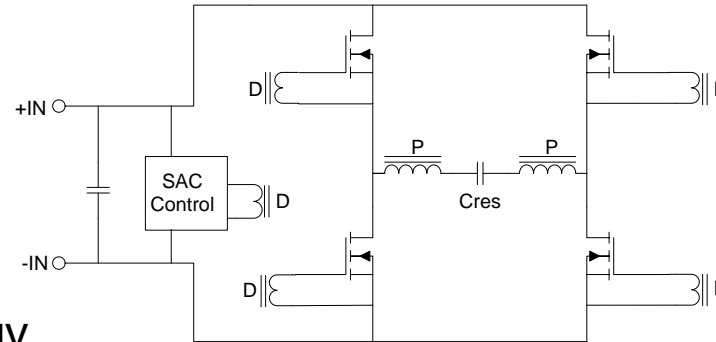
- Regulated = PRM (Regulator) + VTM (Transformer)
 - e.g. 48V_{IN} with 1.2V_{OUT}, 130A





High Efficiency Bus Conversion

- Bus Converter Module (BCM)
 - Isolated, unregulated
 - Voltage transformer / current multiplier
- Sine Amplitude Converter Topology
 - ZVS, ZCS, >1Mhz switching frequency
- 'Full-chip' (1.1in²):
 - 380V: 48V 330W, 96.5%
 - 270V: 28V 235W, 95.4% (MIL-STD 704)
 - 48V : 12V 300W, 95.8%
- 'Half-Chip' (0.55in²)
 - 48V : 12V 120W, 94.6%

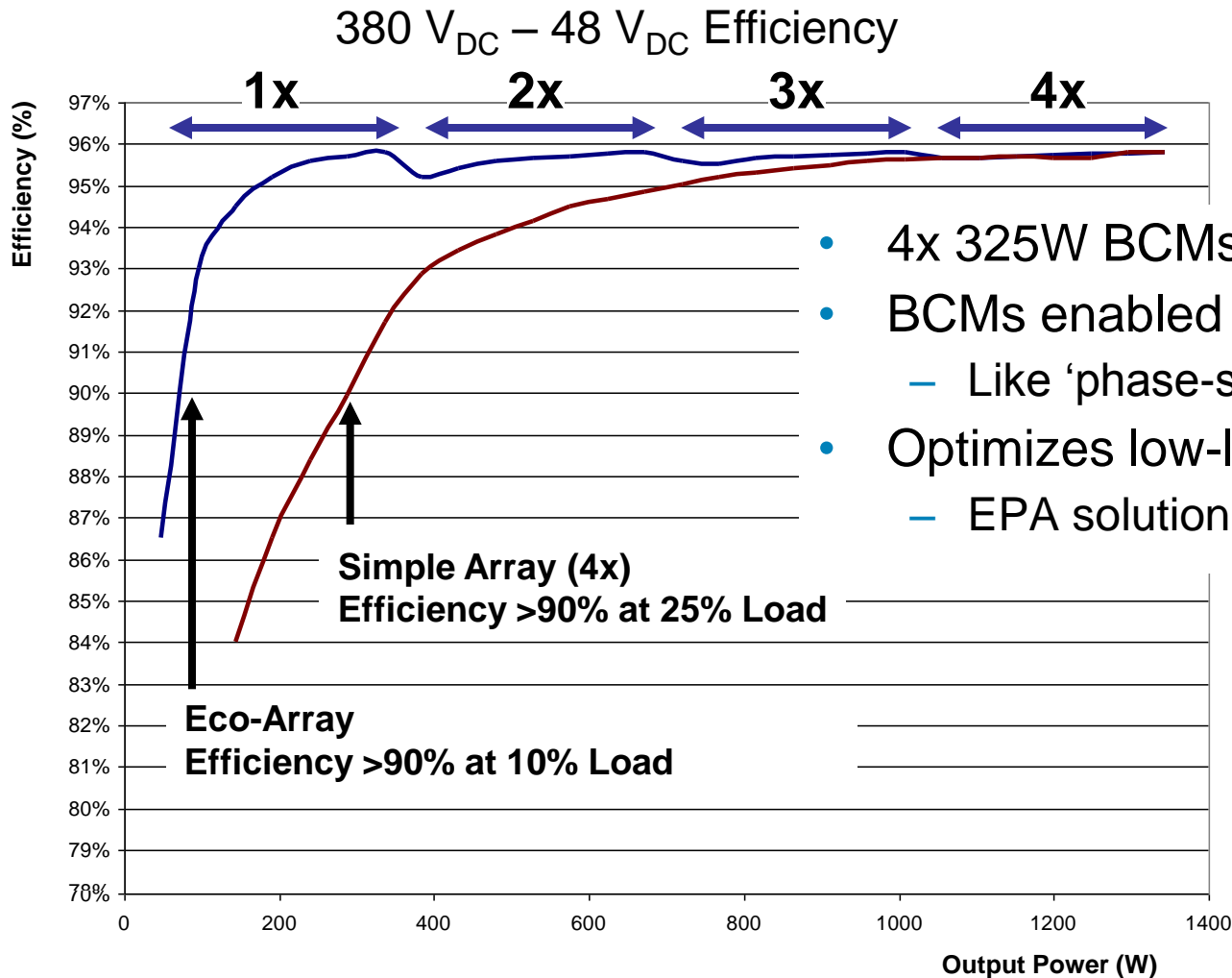


P=Power Transformer
D=Drive Transformer





System Benefits of High Efficiency Converters: Light-Load Efficiency



- 4x 325W BCMs in parallel (1,300W)
- BCMs enabled when needed
 - Like ‘phase-shedding’
- Optimizes low-load efficiency
 - EPA solution





48V to Regulated, <1V Options

- Traditionally, 48V to 'low voltage load' conversion has been a 2-step approach
 - e.g. 48 - 12V with a 'brick' then 12 - xV with a synchronous buck converter
 - As load voltages decrease...
 - Processors now <1V (VR12 spec down to 0.5V), memory <1.2V
- ... the 'duty-cycle' limitations of the synch buck mean that the topology has reached an 'asymptotic' efficiency level
- 12 – 3V is a 4:1 'synchronous FET' to 'control FET' ratio
 - 12 – 0.9V is more than 13:1
- Features like phase shedding, multi-phase switching, higher levels of controller integration, etc. achieve smaller and smaller advances
 - The resonant 'Sine Amplitude Converter' (as used in the BCM), operating on a 'classic' transformer offers the highest efficiency method to convert from 48V directly to a sub-1V level



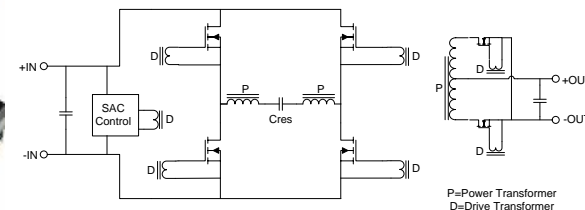
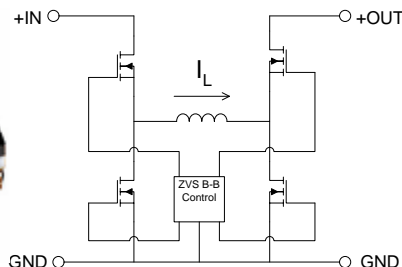
Direct 48V-to-Load Conversion

Pre-Regulator Module (PRM)

- Non-isolated, regulator
- ZVS Buck – Boost Topology
 - ZVS, >1MHz switching
- Performance
 - 400W in 1.1 in²
 - 200W in 0.55 in²
 - Power Density >1,300 W/in³
 - Efficiency >97% at full power
- Input : Unregulated 48V (e.g.)
- Output : Regulated into VTM

Voltage Transformation Module (VTM)

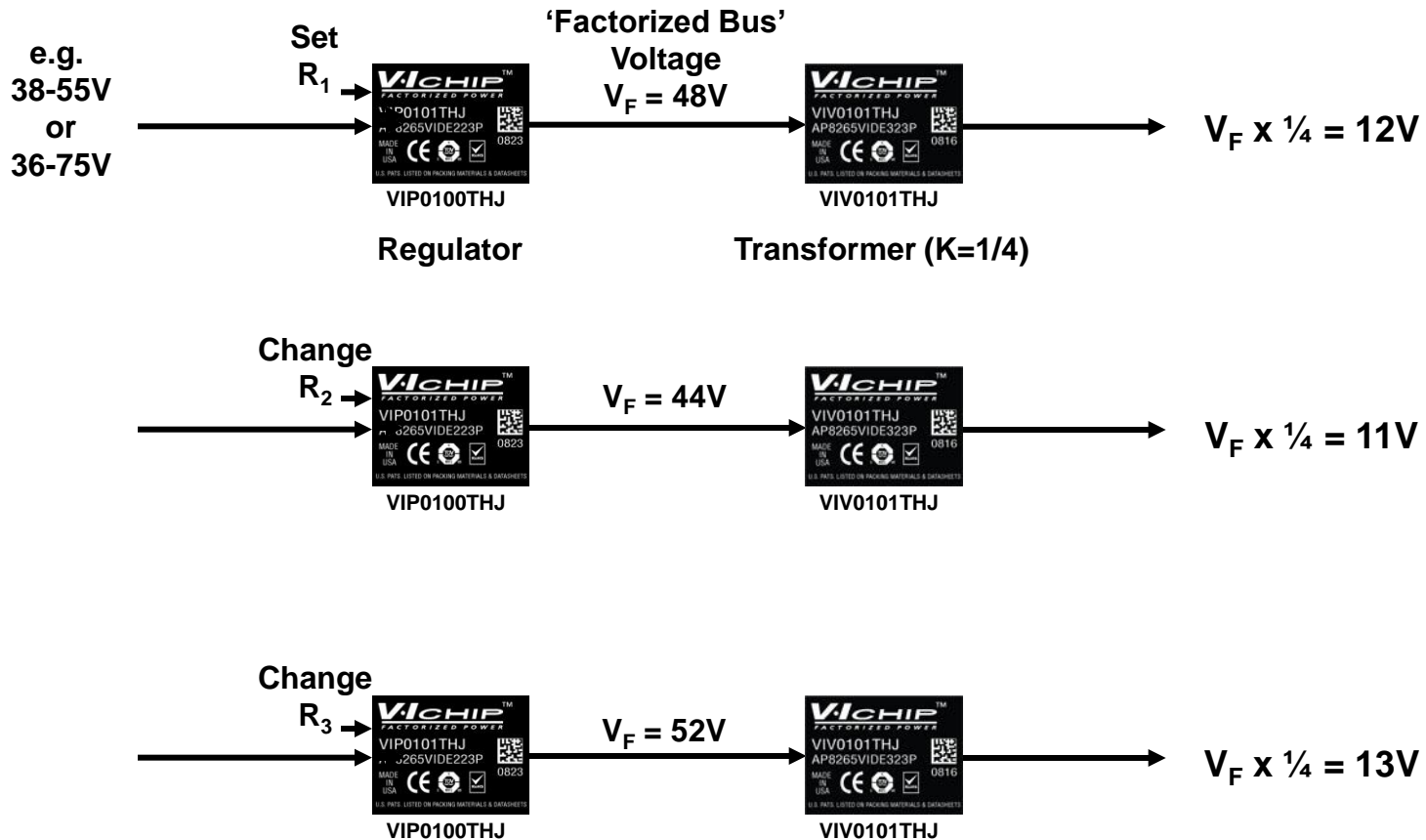
- Isolated, voltage transformer
- Sine Amplitude Converter Topology
 - ZVS, ZCS, >1Mhz switching frequency
- Performance
 - 130A in 1.2 in²
 - 50A in 0.55 in²
 - Current Density >100 A/in²
 - Efficiency >93% at 1.2V, 115A
- Input : Regulated from PRM
- Outputs : 0.15 - 55V, up to 130A



- ***PRM + VTM = Isolated, regulated, voltage transformation direct to load***



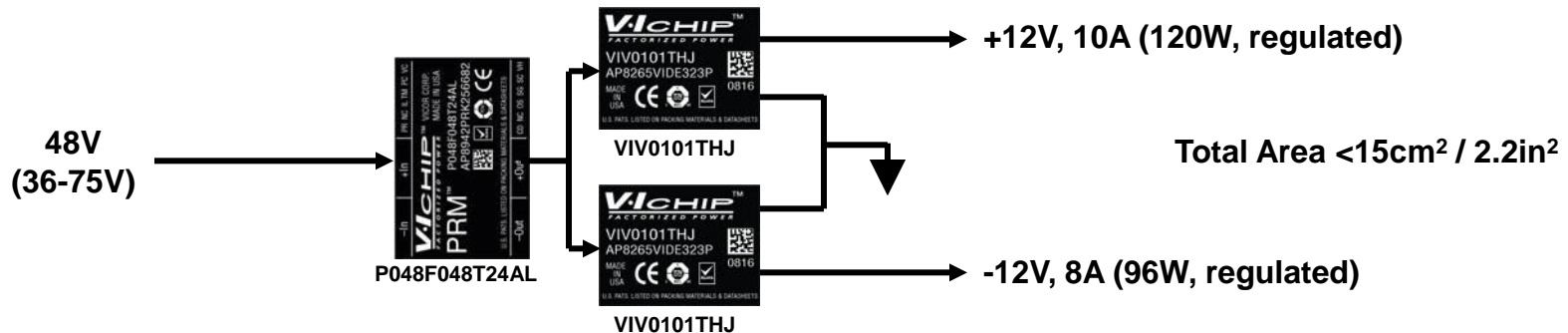
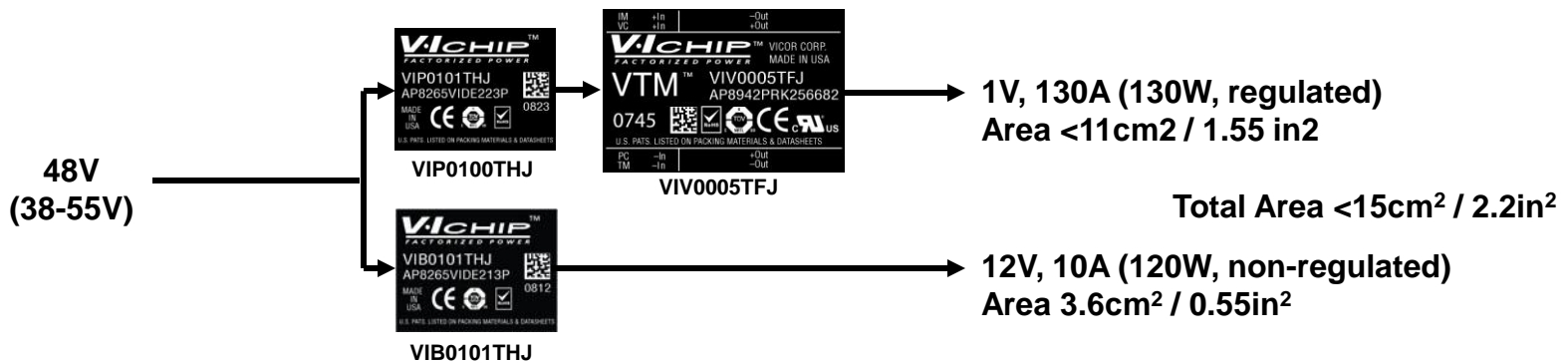
Changing Output Voltage



- Adjust Regulator (PRM) to change 'Factorized bus voltage' (V_F), to change output voltage



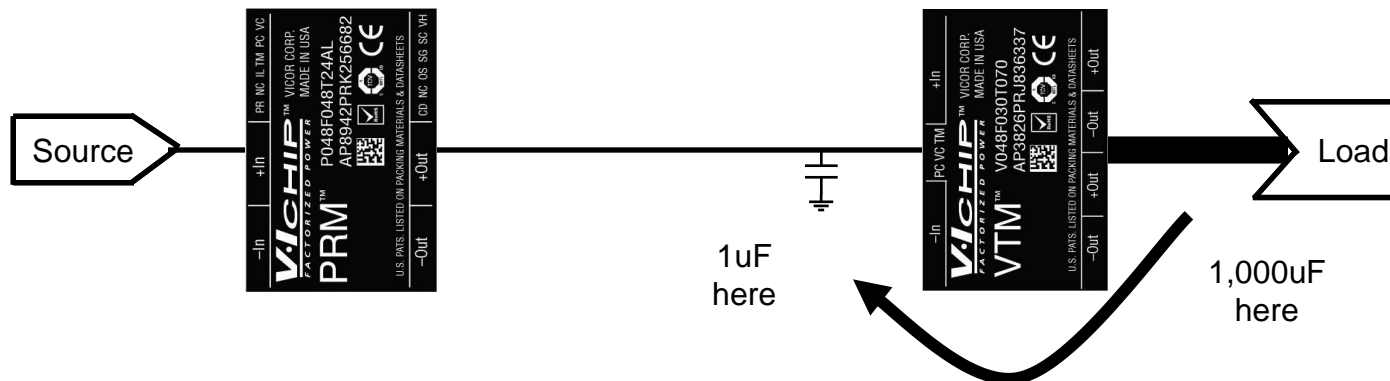
Example Applications





Bulk Capacitance 'Elimination'

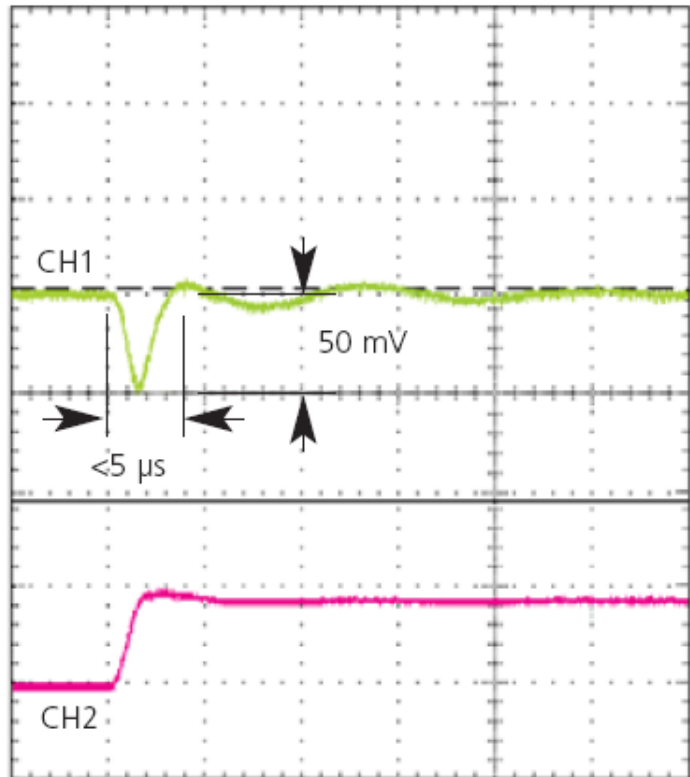
- Direct 48V-to-load conversion with 2 V•I Chips
- PRM can be located remotely
 - Increased space on motherboard / near load
 - Reduced power dissipation at load
- Move POL Capacitance to input of VTM
 - Reduce capacitance by $1/K^2$ (as energy stored in capacitor is $\sim V^2$)
 - Additional space and cost savings





Transient Response

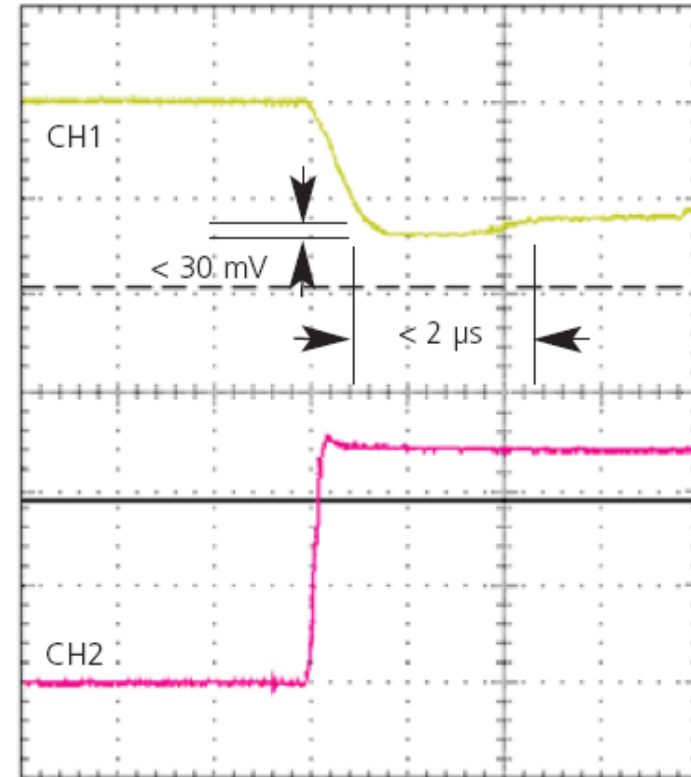
Load Step Recovery



CH1: V_{OUT} 50 mV/div
 CH2: I_{OUT} 50 A/div
 Timebase: 5 μs

$48 V_{IN}$, $1.2 V_{OUT}$, $0-40 A$ at $10 A/\mu\text{s}$
 Less than 50 mV undershoot and recovery
 in $< 5 \mu\text{s}$ using $330 \mu\text{F}$ ceramic C_{OUT} .

Load Line Recovery



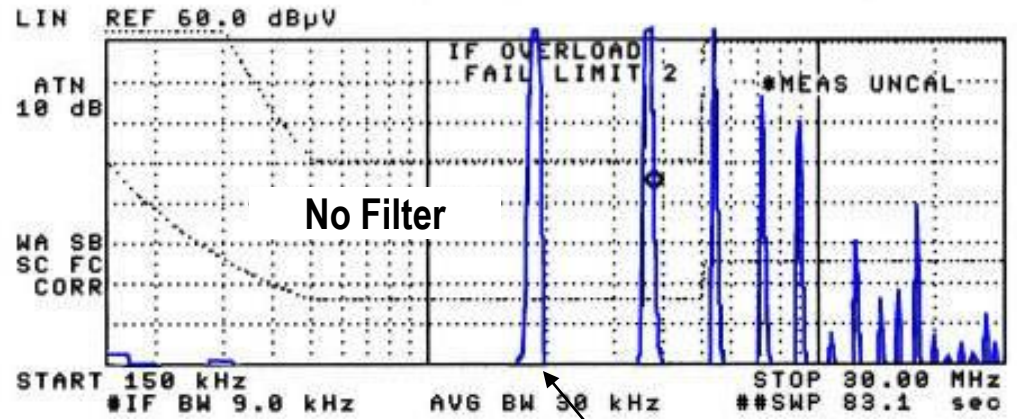
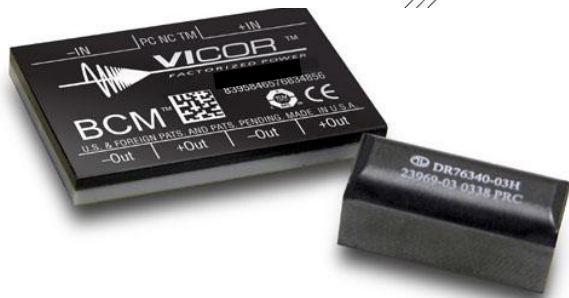
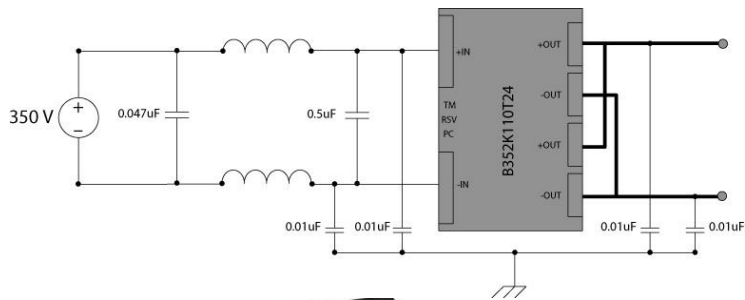
CH1: V_{OUT} 100 mV/div
 CH2: I_{OUT} 40 A/div
 Timebase: 1 μs

$48 V_{IN}$, $1.2 V_{OUT}$, $0-100 A$ at $600 A/\mu\text{s}$
 Less than 30 mV undershoot and recovery
 in $< 2 \mu\text{s}$ using $220 \mu\text{F}$ ceramic C_{OUT} .

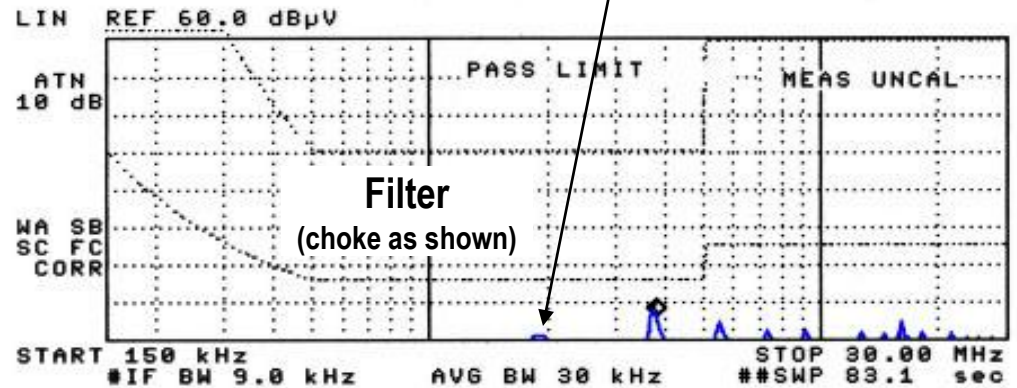


Predictable EMI, Smaller System

- 1.75 MHz switching frequency (effective 3.5 MHz)
 - Easy-to-filter ripple
 - Small, high frequency components
 - High voltage, low current designs
- 'Quiet', low profile powertrain for noise-sensitive, tightly-racked applications (e.g. ATE)



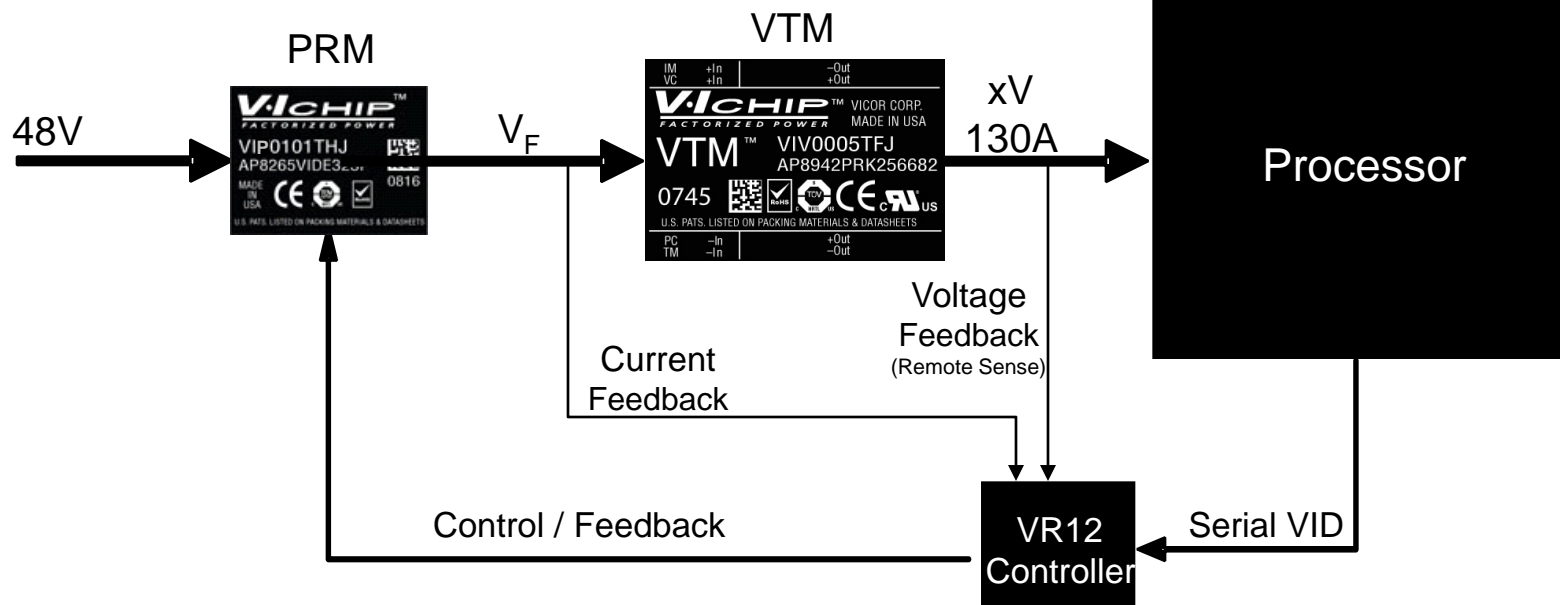
1st fundamental >> 1MHz





Direct 48V-to-Intel Processor (VR12 with FPA)

- ‘Voltage Regulator’ (VR) spec sets voltage to match specific peak performance of individual processors
- FPA is a ‘pure power’ solution
 - Digital or analog loop
 - Any industry standard controller (with access to VID)
 - Re-use existing control / housekeeping solutions





The FPA Advantage

- Applying FPA to higher power systems highlights the size, efficiency and value of the V•I Chips

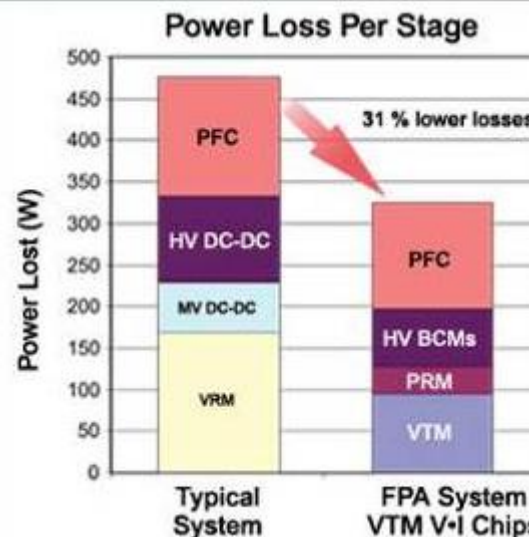
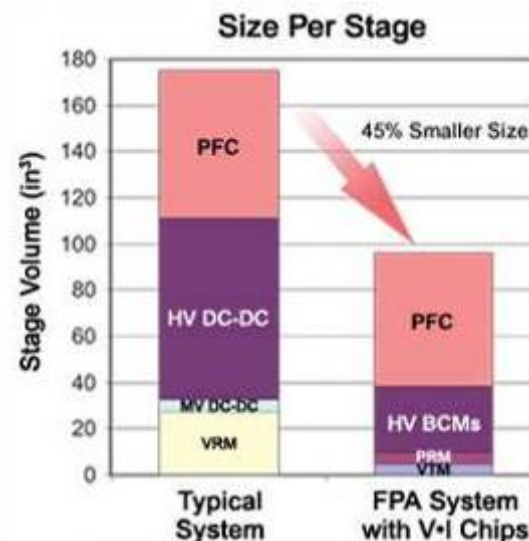
- Efficiency** ↑ 9%
- Power Loss** ↓ 45%
- Size** ↓ 45%

- Save **Money**:
 - \$30 per year, per processor
 - \$600,000 per year, per datacenter

- Save **Energy** (Oil)
 - 2,600 barrels per year, per datacenter

- Save the **Environment**
 - 2,800 tons CO₂ per year, per datacenter

Typical 20,000 processors per data center





380V_{DC} to 12V: Cray 'CX1' / Dell 'LC'



380V → 12V Conversion
Hot-swap, In-rush, etc.

2x 300W HV BCMs

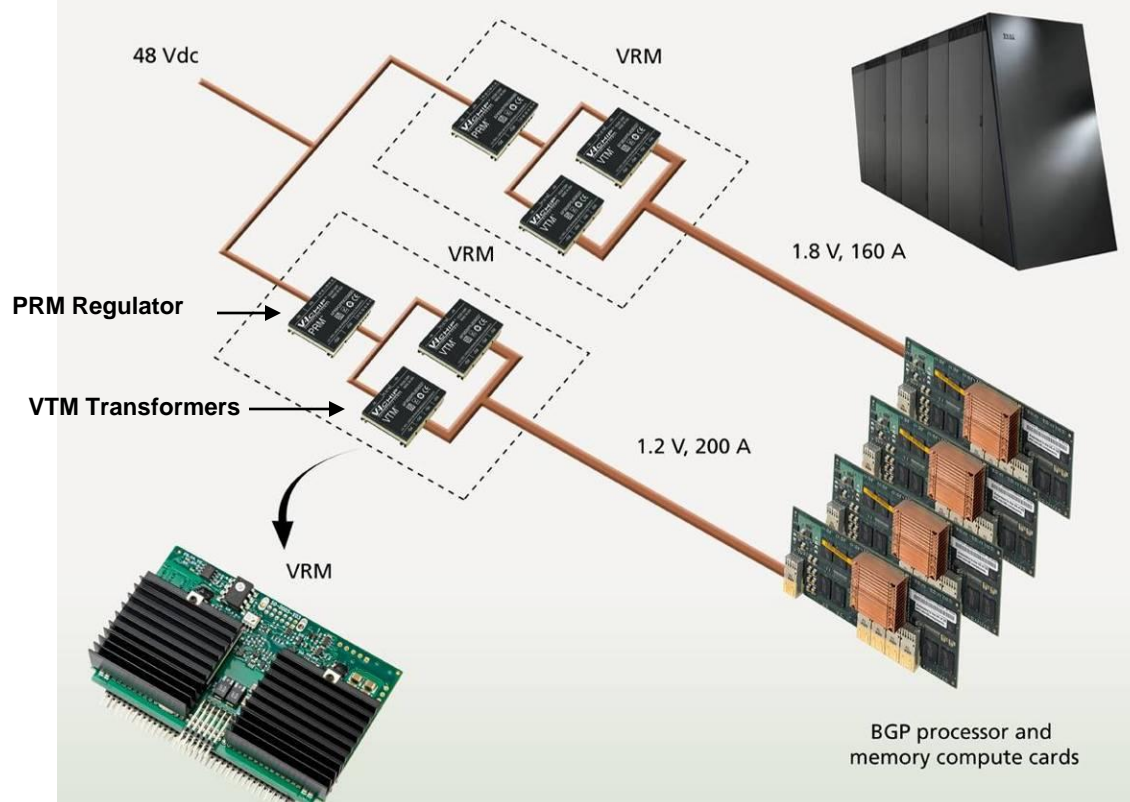
600W, 380V_{IN} → 12V_{OUT} at 95.5%

110/220 VAC → 380 V_{DC} → 12 V → Processor, etc.



48V to Processor / Memory: IBM Blue Gene/P

- Current density of $>90 \text{ A/in}^2$
- Blue Gene/P with Vicor holds 12 of the top 20 in the Green500 (Mflops/Watt)

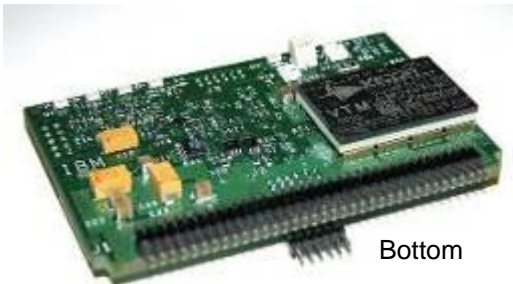




IBM Blue Gene/P



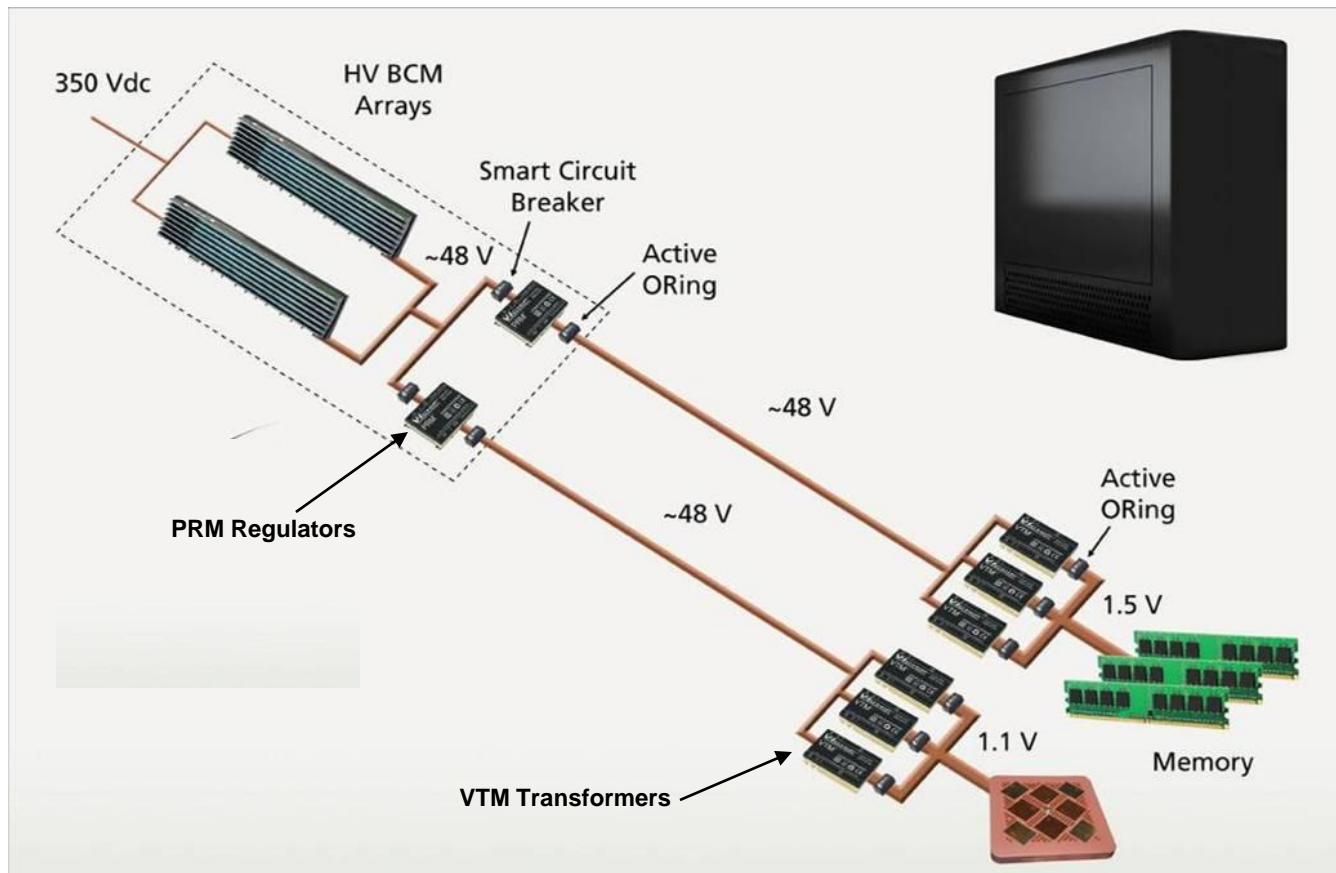
- Direct 48V-to-load Conversion
 - 1x PRM +2x VTMs per card
 - $48V_{IN}$, $1.2V_{OUT}$, 200A for processors
 - $48V_{IN}$, $1.8V_{OUT}$, 160A for memory





HVDC to Processor / Memory: IBM Power 7

- PRM regulators ‘factorized’ away from VTM transformers
 - High efficiency distribution, high efficiency power conversion at load





V.I Chips in p7-IH

DCCA
(BCMs, PRMs)



Node (top)



Node (bottom)
(VTMs)





In Summary: High Efficiency Power Architectures

- The keys:
 - High(er) voltage distribution
 - High efficiency power converters
 - Intelligent exploitation of key features to achieve system benefits
- FPA and V•I Chips
 - Highest system efficiency
 - Smallest power system size